Amendment to the Claims:

The claims under examination in this application, including their current status and changes made in this paper, are respectfully presented.

1 (original). A method for timing recovery of a digital signal in a telecommunications receiver, comprising:

tracking a plurality of coefficients in a tracking buffer for timing drift,

centering the plurality of coefficients in the tracking buffer,

filtering, through an equalizer, the digital signal with the plurality of coefficients, and

updating the plurality of coefficients in the tracking buffer.

2 (currently amended). A method for timing recovery of a digital signal according to claim 1, wherein:

the step of tracking the [a] plurality of coefficients further comprises,

summing a set of left coefficients,

summing a set of center coefficients,

summing a set of right coefficients,

comparing the set of left coefficients, the set of center coefficients, and the set of right coefficients to obtain a set with the greatest weighting; and

the step of centering the plurality of coefficients further comprises centering the plurality of coefficients about the set with the greatest weighting,

filtering, through an equalizer, the digital signal with the plurality of coefficients, and

updating the plurality of coefficients in the tracking buffer.

3 (original). A method for timing recovery of a digital signal in a telecommunications receiver, comprising:

splitting the digital signal into an in-phase input signal and a quadrature input signal,

tracking a plurality of coefficients in a tracking buffer for timing drift, wherein the coefficients are in-phase coefficients,

centering the plurality of in-phase coefficients in the tracking buffer,

centering the plurality of quadrature coefficients in the tracking buffer,

filtering, through an in-phase equalizer, the in-phase signal with the plurality of in-phase coefficients,

filtering, through a quadrature equalizer, the quadrature signal with the plurality of quadrature coefficients,

updating the plurality of in-phase coefficients in the tracking buffer, and

updating the plurality of quadrature coefficients in the tracking buffer.

Cl Cont.

4 (original). A method for timing recovery according to claim 3, further comprising:

tracking a plurality of coefficients in a tracking buffer for timing drift, wherein the coefficients are quadrature coefficients.

5 (original). A timing recovery device for processing a digital signal, comprising:

an equalizer for processing said digital signal,

a filter buffer for storing a plurality of equalizer coefficients to be applied to said equalizer, and

a buffer manager for tracking the equalizer coefficients within the filter buffer, and for shifting the coefficients within the filter buffer such that the coefficients remain substantially centered within the filter buffer.

6 (original). A timing recovery device according to claim 5, wherein the tracking buffer further comprises:

a data tracking buffer for storing a portion of said signal, and

a coefficient tracking buffer for storing said equalizer coefficients.

7 (original). A timing recovery device according to claim 5, further comprising:

a data tracking buffer for pointing to said portion of said signal stored in said tracking buffer, and

a coefficient tracking buffer for pointing to said equalizer coefficients.

8 (canceled).

9 (canceled).

10 (canceled).

Cl Cont.

11 (previously added). A receiver, comprising:

an analog-to-digital converter, for converting a received analog signal to digital samples;

an adaptive equalizer, for applying a digital filter to a sequence of the digital samples using a sequence of continually updated filter coefficients;

a tracking buffer, for storing the sequence of filter coefficients, the tracking buffer having a length longer than the length of the sequence of filter coefficients used by the adaptive equalizer; and

buffer management circuitry, for tracking movement, within the tracking buffer, of the position of those filter coefficients having the highest values, and for shifting the position of the sequence of filter coefficients within the tracking buffer, so that those filter coefficients having the highest values are in a central portion of the sequence.

12 (previously added). The receiver of claim 11, wherein the tracking buffer comprises:

a data sample tracking buffer, for storing data samples including the sequence of digital samples;

a tap weight tracking buffer, for storing filter coefficients including the sequence of filter coefficients.

13 (previously added). The receiver of claim 12, wherein the sequence of digital samples is stored in a data filter buffer within the data sample tracking buffer;

wherein the sequence of filter coefficients is stored in a coefficient filter buffer within the tap weight tracking buffer;

wherein the buffer management circuitry shifts the position of the coefficient filter buffer within the tap weight tracking buffer so that those filter coefficients having the highest values are in a central portion of the sequence of filter coefficients;

and wherein the buffer management circuitry shifts the position of the data filter buffer within the data sample tracking buffer corresponding to shifts in the position of the coefficient filter buffer within the tap weight tracking buffer.

Cont.

14 (previously added). The receiver of claim 12, further comprising:

a data filter buffer for storing a value pointing to the location of the sequence of digital samples within the data sample tracking buffer; and

a coefficient filter buffer for storing a value pointing to the location of the sequence of filter coefficients within the tap weight tracking buffer;

wherein the buffer management circuitry adjusts the value stored in the coefficient filter buffer so that those filter coefficients having the highest values are in a central portion of the sequence of filter coefficients;

and wherein the buffer management circuitry adjusts the value stored in the data filter buffer corresponding to adjustment of the value stored in the coefficient filter buffer.

15 (previously added). The receiver of claim 11, wherein the adaptive equalizer comprises:

an in-phase adaptive equalizer for applying a digital filter to a sequence of the digital samples corresponding to an in-phase component of the analog signal, using a sequence of continually updated in-phase filter coefficients;

a quadrature-phase adaptive equalizer for applying a digital filter to a sequence of the digital samples corresponding to a quadrature-phase component of the analog signal, using a sequence of continually updated quadrature-phase filter coefficients;

wherein the tracking buffer is for storing the sequence of in-phase filter coefficients and the sequence of quadrature-phase filter coefficients; and

wherein the buffer management circuitry is for tracking movement of the position within the tracking buffer of both the in-phase and quadrature-phase filter coefficients having the highest values, and for shifting the position of both the in-phase and quadrature-phase sequences of filter coefficients.